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(12) **United States Patent**
Poo et al.

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(54) **METHOD FOR PACKAGING CIRCUITS**

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(65) **Prior Publication Data**

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Related U.S. Application Data

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(30) **Foreign Application Priority Data**

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(51) **Int. Cl.**
H05K 3/30 (2006.01)
H01L 21/56 (2006.01)
(Continued)

(52) **U.S. Cl.**
CPC ***H01L 21/56*** (2013.01); ***H01L 21/6835*** (2013.01); ***H01L 22/00*** (2013.01);
(Continued)

(58) **Field of Classification Search**
CPC H01L 21/6835; H01L 25/0657; H01L 25/50; H01L 21/56; H01L 22/00; H01L 24/05; H01L 2924/12042; H01L 2221/68345; H01L 2225/06524; H01L 2225/06541; H01L 2225/06551; H01L 2225/06575; H01L 2924/00; Y10T 29/49146; Y10T 29/49169; Y10T 29/49794; Y10T 29/49128; Y10T 29/49167; Y10T 29/49155; Y10T 29/49144; Y10T 29/49165; Y10T 29/4913
USPC 29/830, 832, 841, 842, 846; 257/753, 257/783; 438/113, 127, 460
See application file for complete search history.

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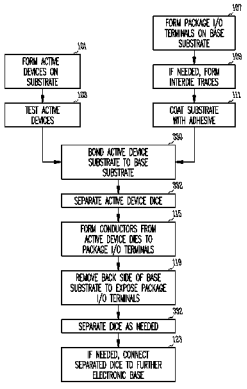
(57) **ABSTRACT**

A method for packaging integrated circuit chips (die) is described that includes providing a base substrate with package level contacts, coating a base substrate with adhesive, placing dies on the adhesive, electrically connecting the die to the package level contacts, and removing the backside of the base substrate to expose the backside of the package level contacts. Accordingly, an essentially true chip scale package is formed. Multi-chip modules are formed by filling gaps between the chips with an encapsulant. In an embodiment, chips are interconnected by electrical connections between package level contacts in the base substrate. In an embodiment, substrates each having chips are adhered back-to-back with through vias formed in aligned saw streets to interconnect the back-to-back chip assembly.

7 Claims, 13 Drawing Sheets



(51) **Int. Cl.**

H01L 21/683	(2006.01)
H01L 25/065	(2006.01)
H01L 25/00	(2006.01)
H01L 21/66	(2006.01)
H01L 23/00	(2006.01)

(52) **U.S. Cl.**

CPC ***H01L 24/05*** (2013.01); ***H01L 25/0657*** (2013.01); ***H01L 25/50*** (2013.01); *H01L 2221/68345* (2013.01); *H01L 2225/06524* (2013.01); *H01L 2225/06541* (2013.01); *H01L 2225/06551* (2013.01); *H01L 2225/06575* (2013.01); *H01L 2924/12042* (2013.01); *H01L 2924/14* (2013.01); *Y10T 29/4913* (2015.01); *Y10T 29/49128* (2015.01); *Y10T 29/49144* (2015.01); *Y10T 29/49146* (2015.01); *Y10T 29/49155* (2015.01); *Y10T 29/49165* (2015.01); *Y10T 29/49167* (2015.01); *Y10T 29/49169* (2015.01); *Y10T 29/49794* (2015.01)

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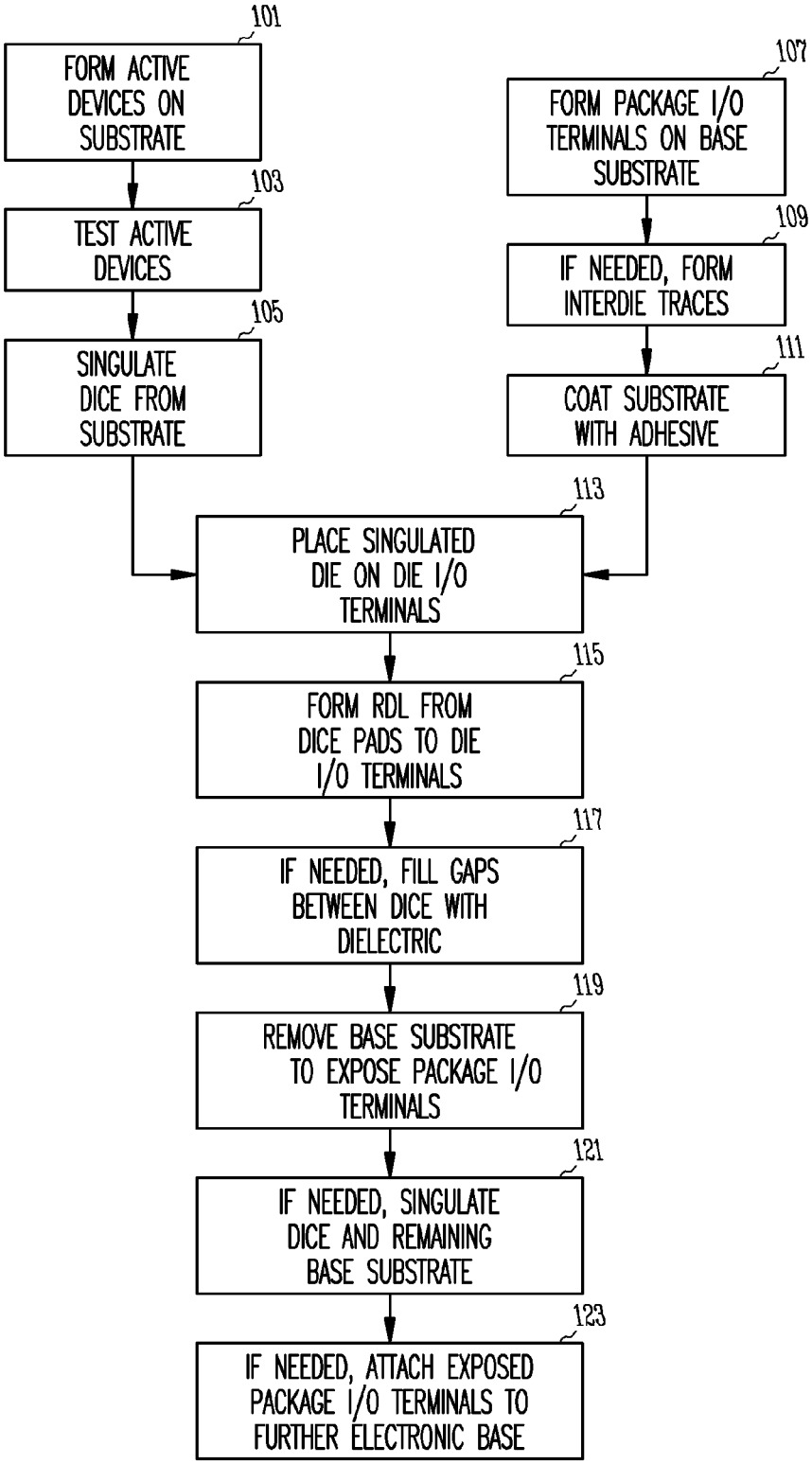
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TEST ACTIVE DEVICES
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SINGULATE DICE FROM SUBSTRATE
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FORM PACKAGE I/O TERMINALS ON BASE SUBSTRATE
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IF NEEDED, FORM INTERDIE TRACES
111
COAT SUBSTRATE WITH ADHESIVE
113
PLACE SINGULATED DIE ON DIE I/O TERMINALS
115
FORM RDL FROM DICE PADS TO DIE I/O TERMINALS
117
IF NEEDED, FILL GAPS BETWEEN DICE WITH DIELECTRIC
119
REMOVE BASE SUBSTRATE TO EXPOSE PACKAGE I/O TERMINALS
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IF NEEDED, SINGULATE DICE AND REMAINING BASE SUBSTRATE
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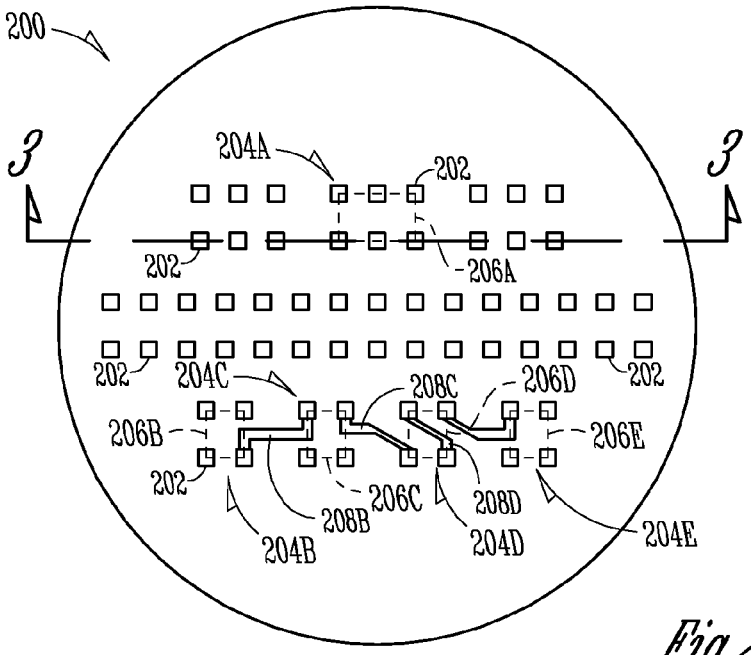
IF NEEDED, ATTACH EXPOSED PACKAGE I/O TERMINALS TO FURTHER ELECTRONIC BASE

Fig. 1



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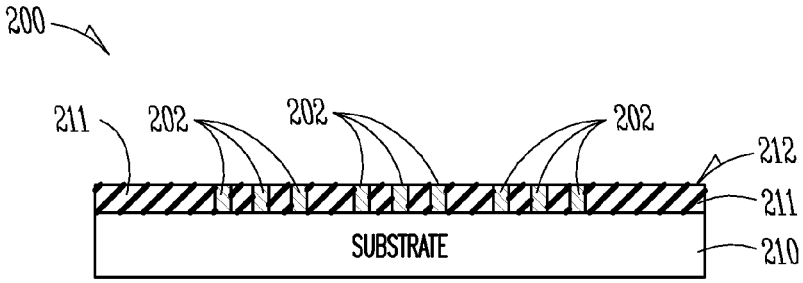

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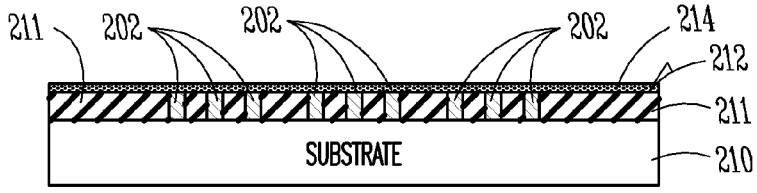

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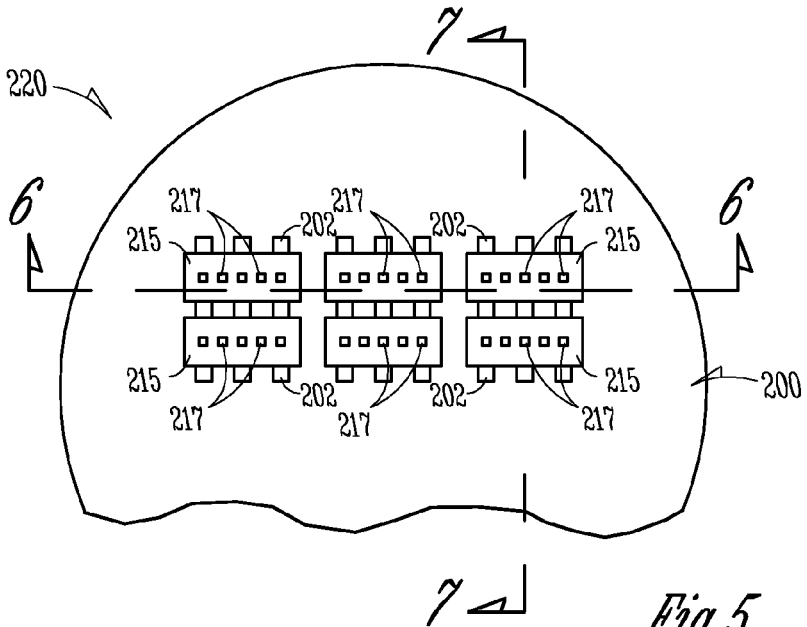

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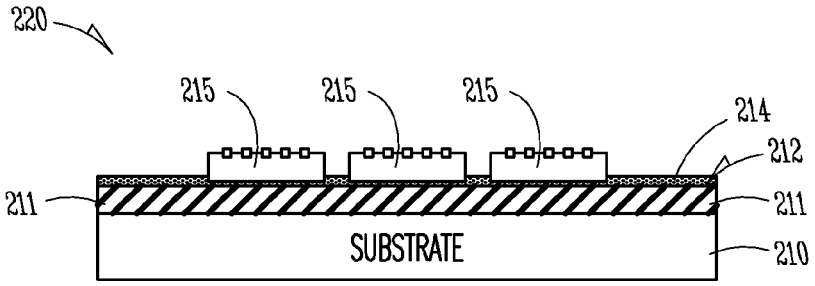

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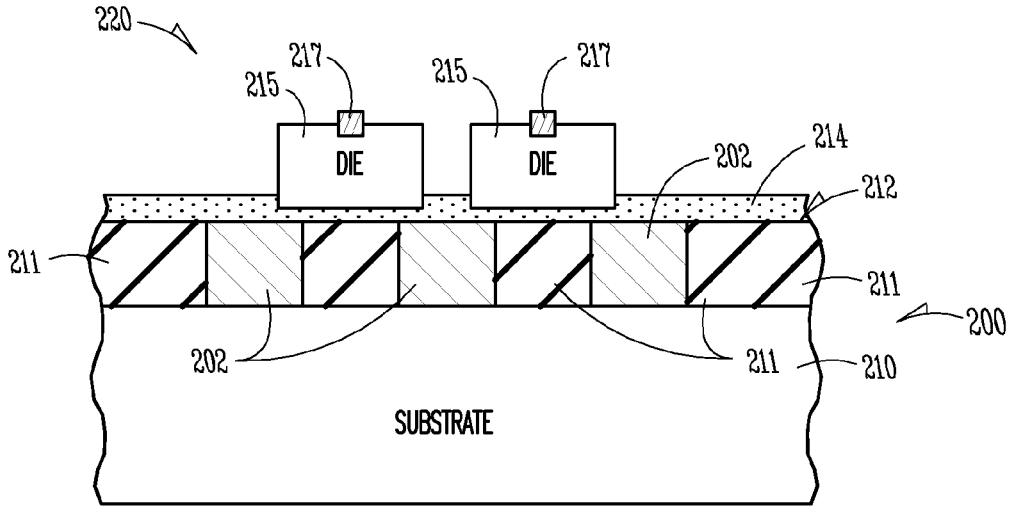

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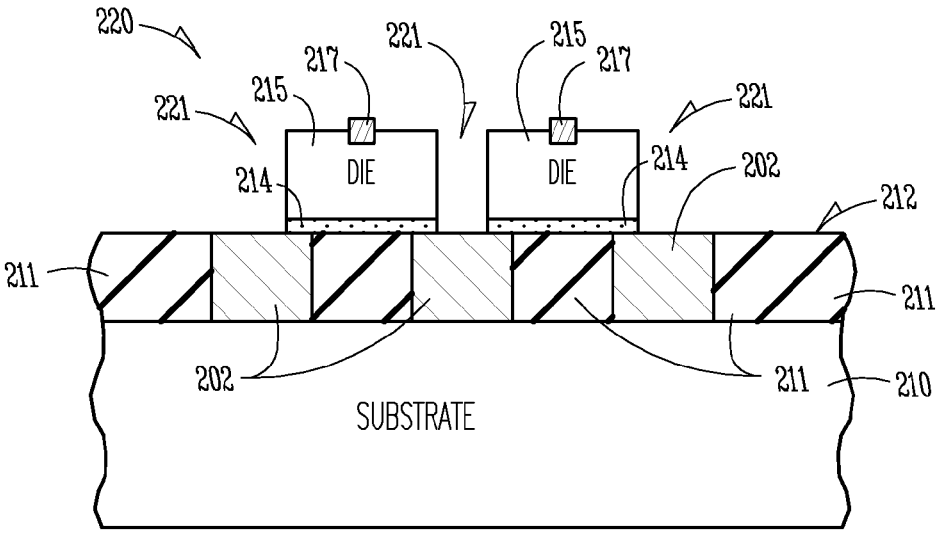
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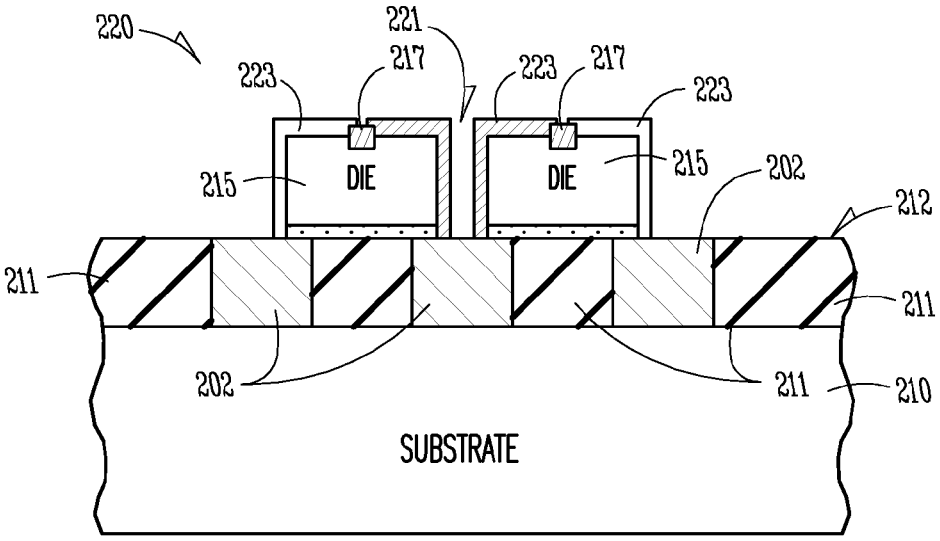
SUBSTRATE

Fig. 8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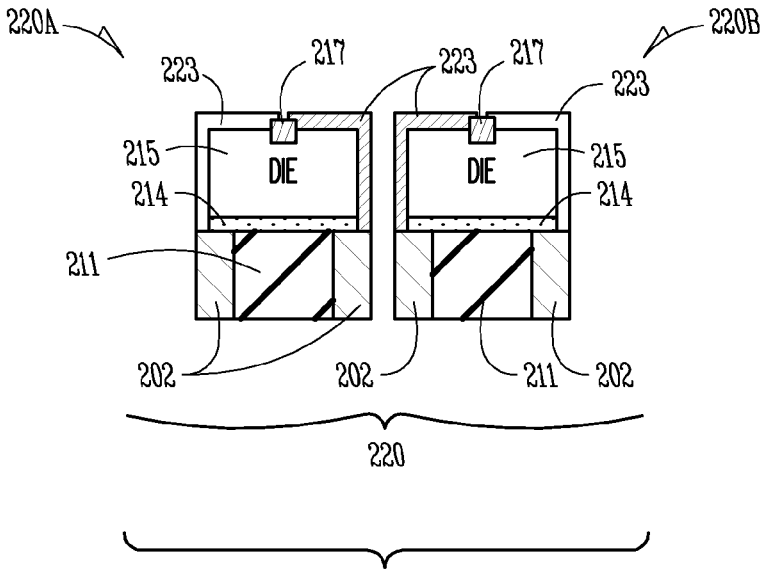
SUBSTRATE

Fig. 9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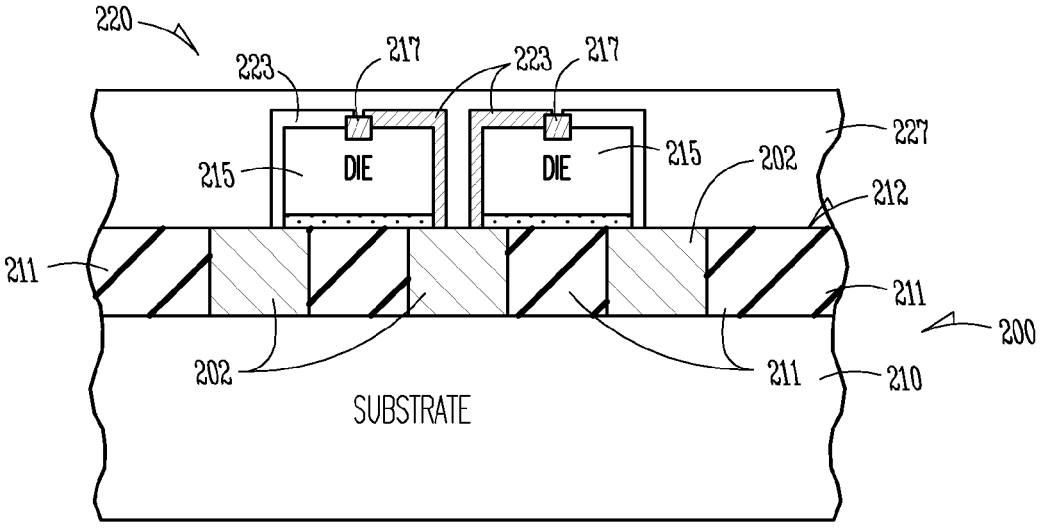
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SUBSTRATE

Fig. 11

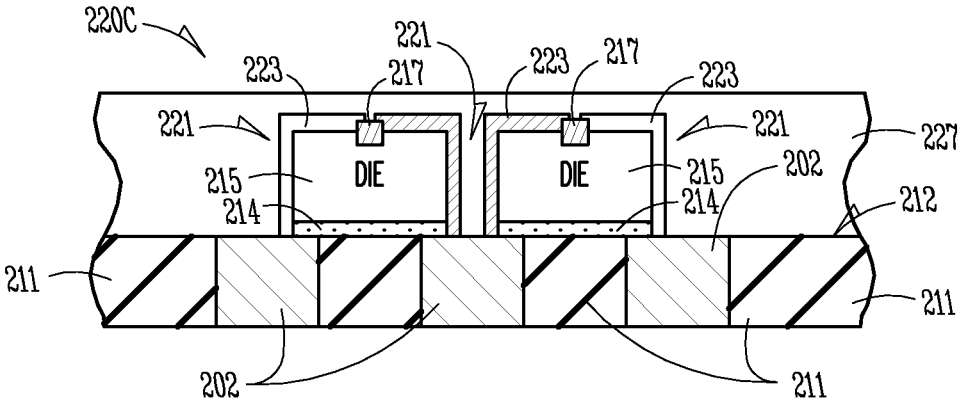
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Fig. 12

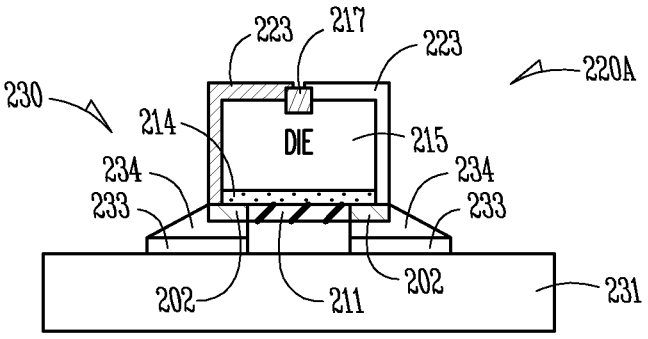
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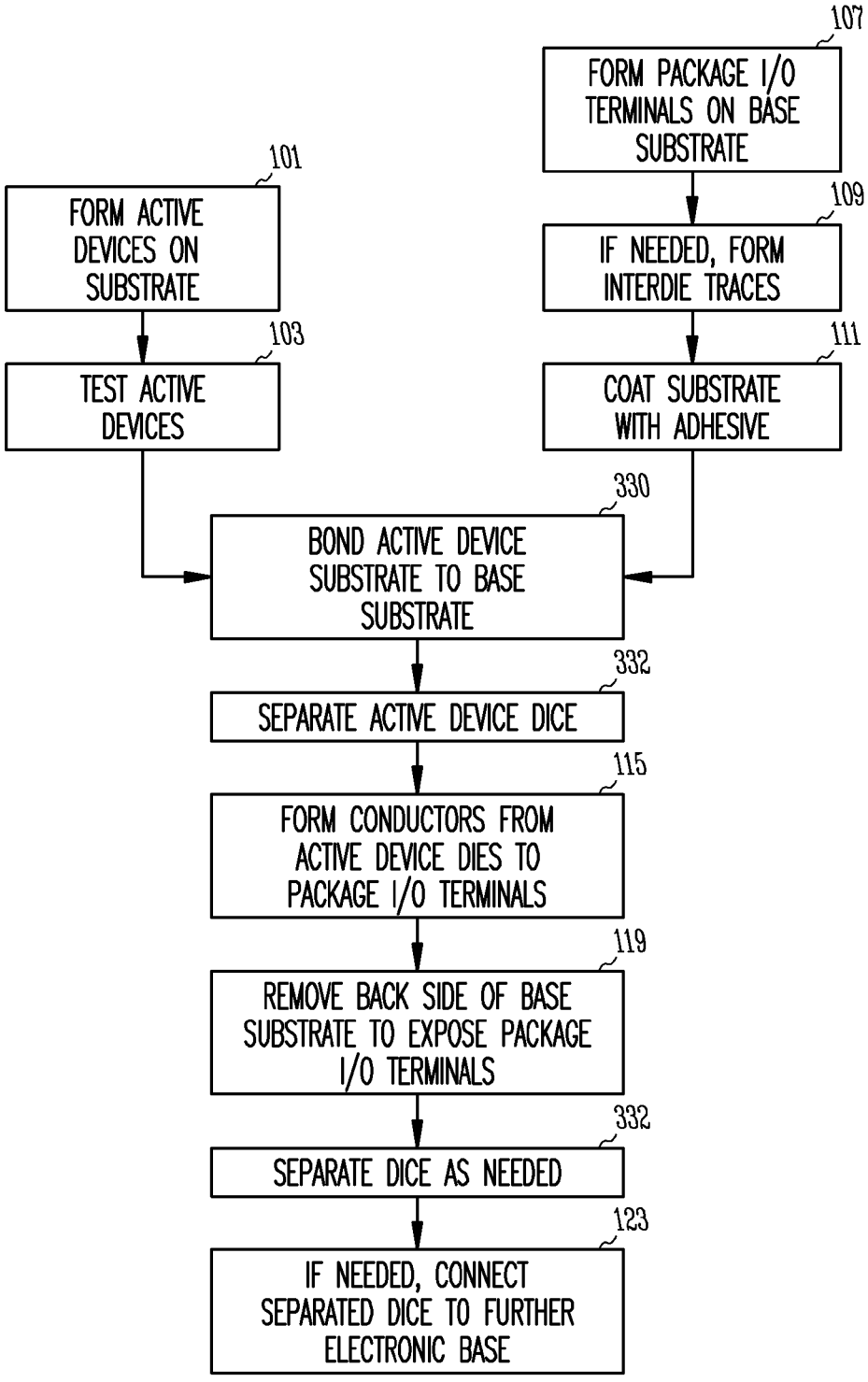
Fig. 13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IF NEEDED, FORM INTERDIE TRACES
103
TEST ACTIVE DEVICES
111
COAT SUBSTRATE WITH ADHESIVE
330
BOND ACTIVE DEVICE SUBSTRATE TO BASE SUBSTRATE
332
SEPARATE ACTIVE DEVICE DICE
115
FORM CONDUCTORS FROM ACTIVE DEVICE DIES TO PACKAGE I/O TERMINALS
119
REMOVE BACK SIDE OF BASE SUBSTRATE TO EXPOSE PACKAGE I/O TERMINALS
332
SEPARATE DICE AS NEEDED
123
IF NEEDED, CONNECT SEPARATED DICE TO FURTHER ELECTRONIC BASE

Fig. 14

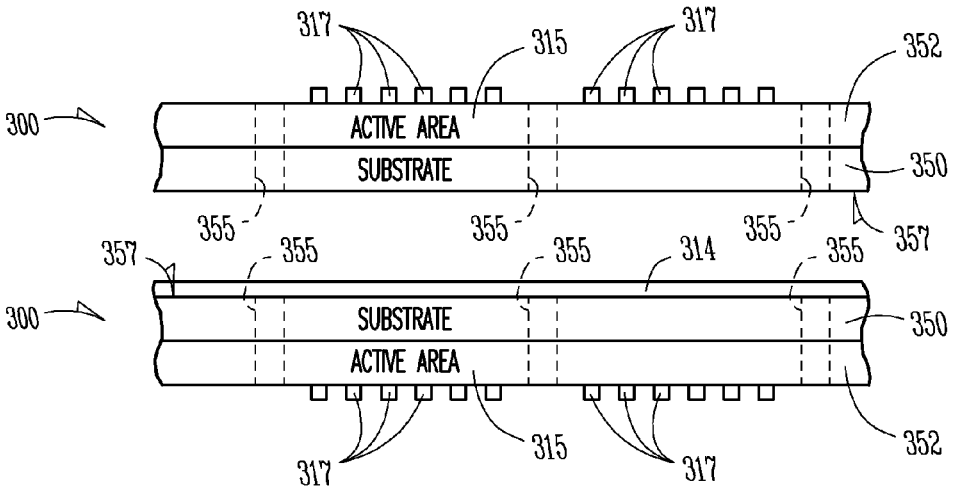
317
315
317
352
300
ACTIVE AREA
SUBSTRATE
350
355
355
355
357
357
355
355
314
355
300
SUBSTRATE
ACTIVE AREA
350
317
315
317
352

Fig. 15

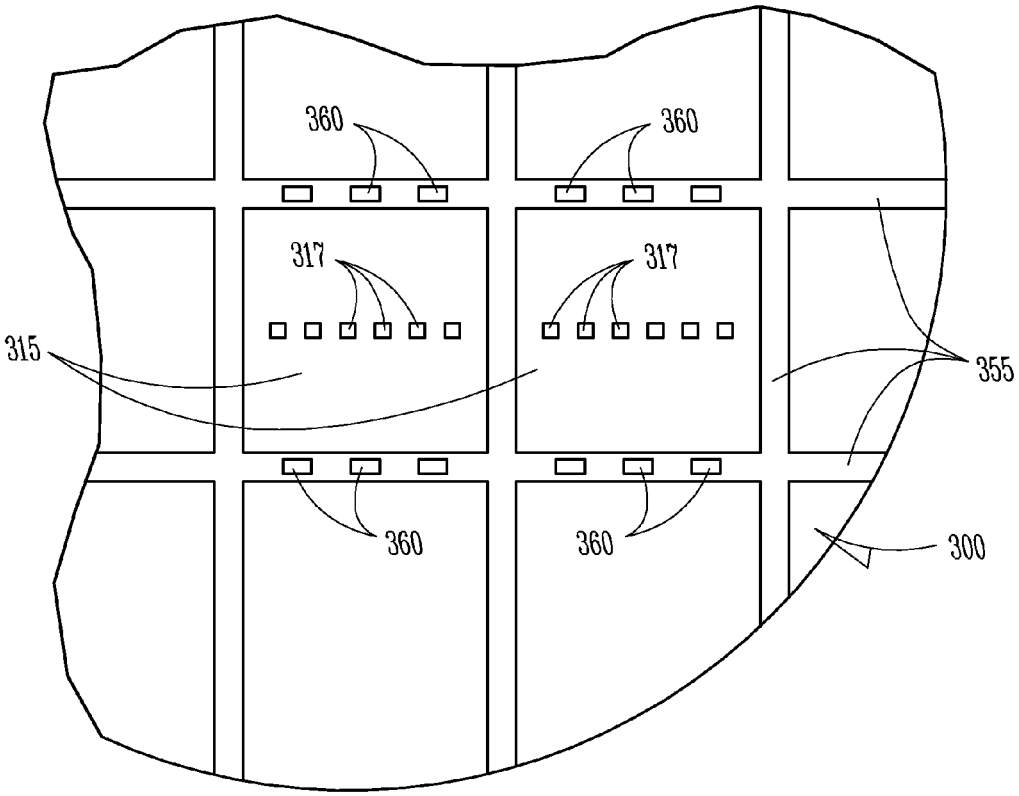
360
360
317
317
315
355
360
360
300

Fig. 16

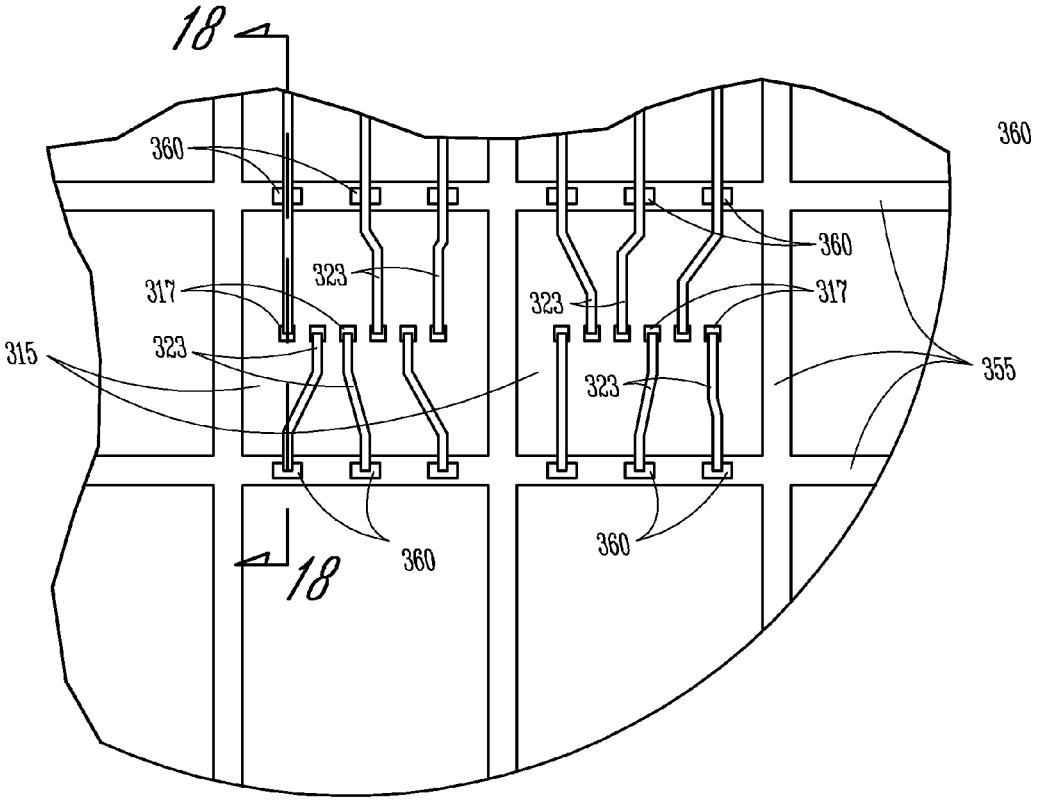
18
360
360
360
317
323
323
317
315
323
355
323
360
360
18

Fig. 17

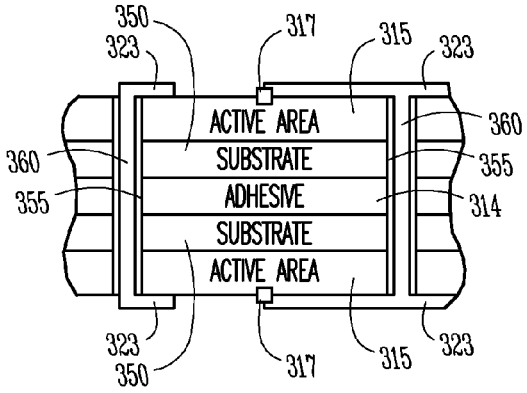
350
323
317
315
323
ACTIVE AREA
SUBSTRATE
ADHESIVE
SUBSTRATE
ACTIVE AREA
360
355
314
360
355
323
350
317
315
323

Fig. 18

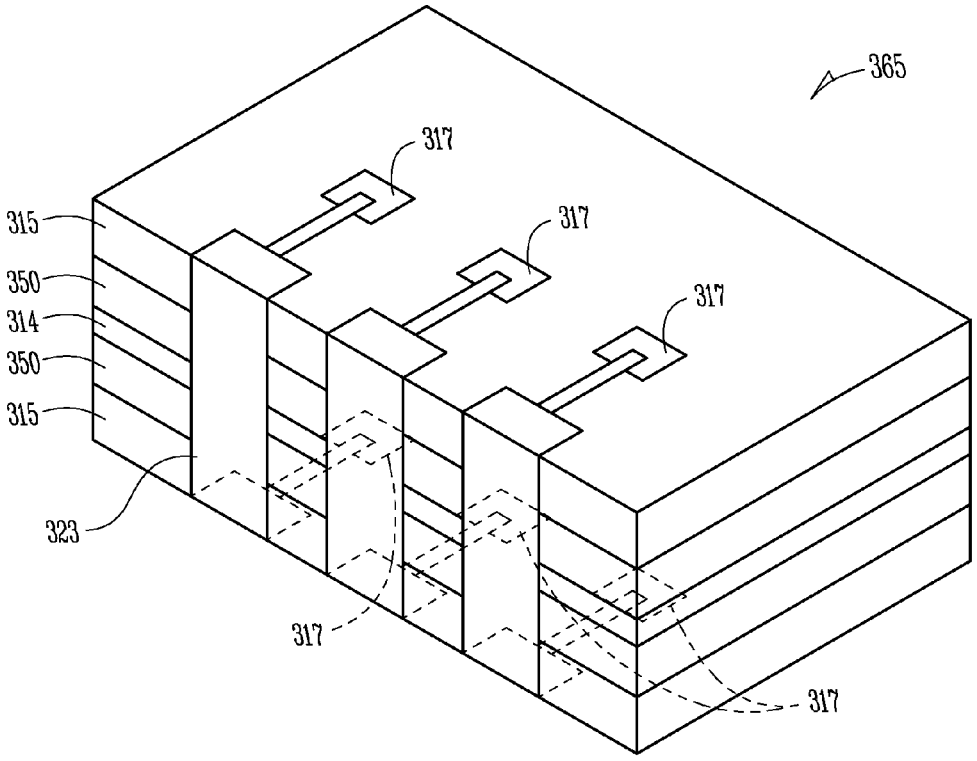
365
317
317
317
315
350
314
350
315
323
317
317

Fig. 19

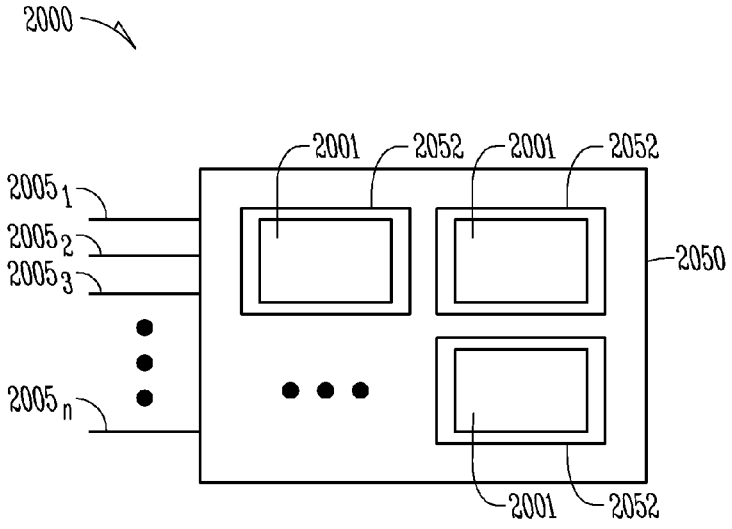
2000
2001
2052
2001
2052
2005_1
2005_2
2005_3
2005_n
2050
2001
2052

Fig. 20

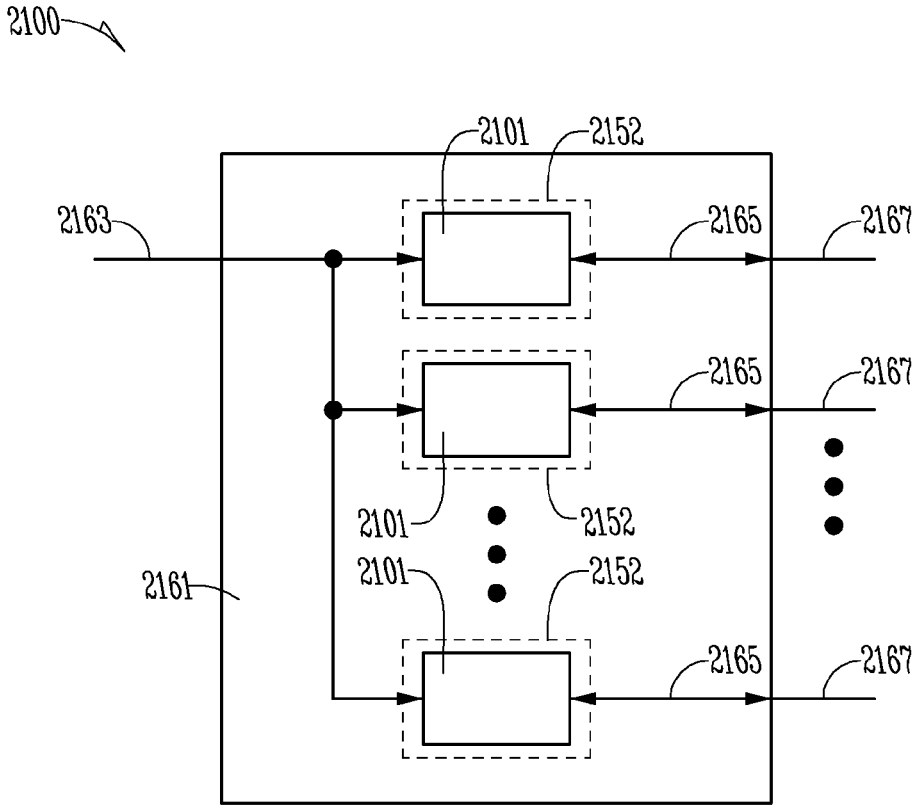
2100
2101
2152
2163
2165
2167
2165
2167
2101
2152
2161
2101
2152
2165
2167

Fig.21

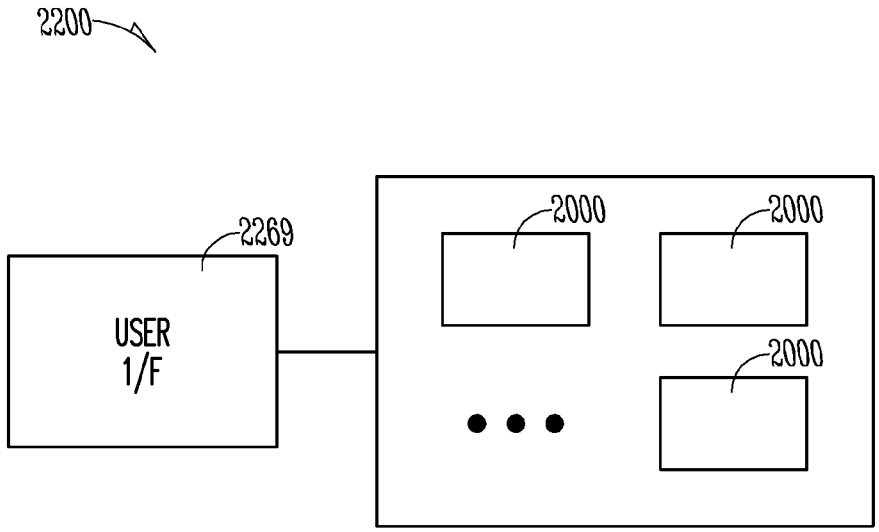
2200
2269
USER
1/F
2000
2000
2000

Fig.22

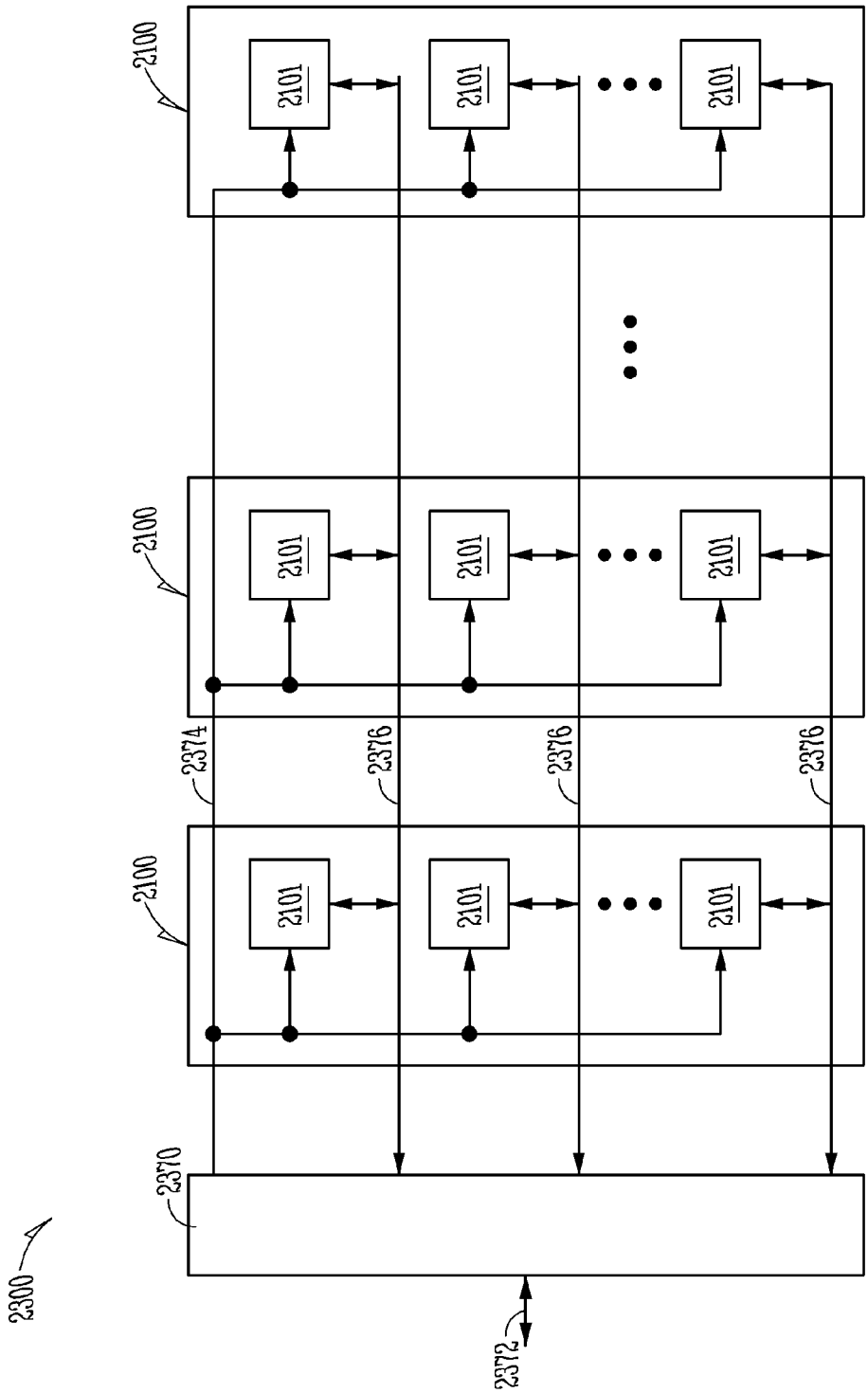
2300
2370
2372
2374
2376
2376
2376
2100
2100
2100
2101
2101
2101
2101
2101
2101
2101
2101
2101

Fig.23

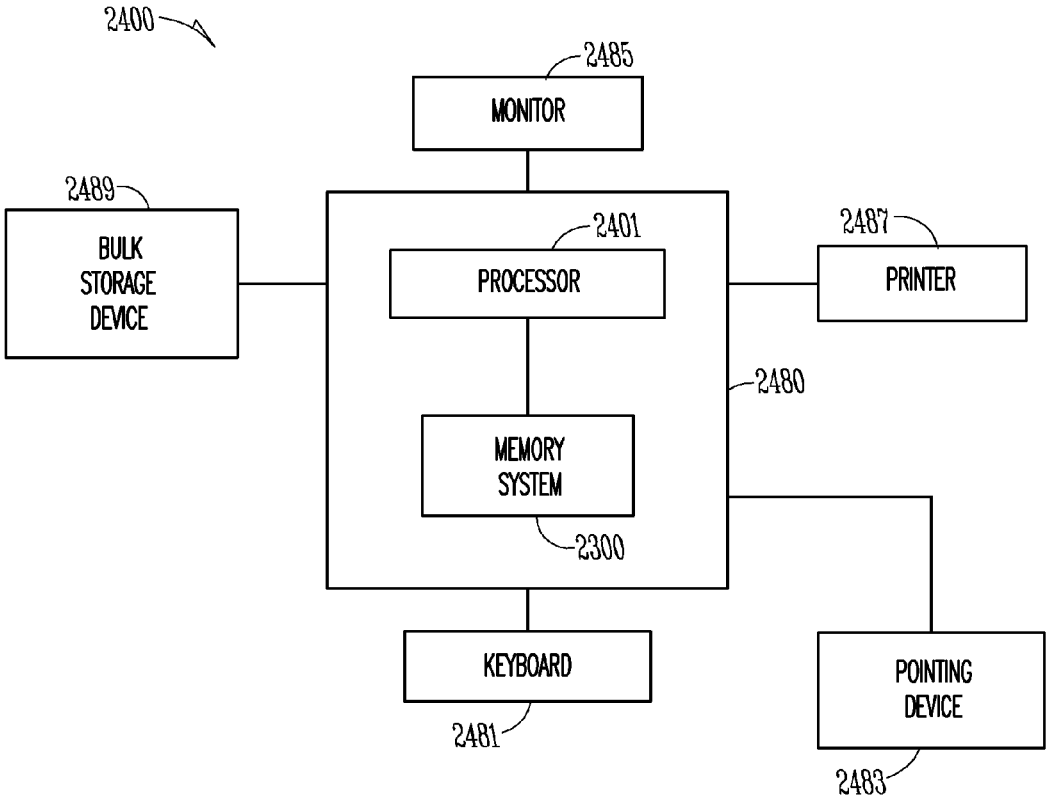
2400
2485
MONITOR
2489
BULK STORAGE DEVICE
2401
PROCESSOR
2487
PRINTER
2480
MEMORY SYSTEM
2300
KEYBOARD
2481
POINTING DEVICE
2483

Fig. 24

METHOD FOR PACKAGING CIRCUITS

This application is a divisional of U.S. application Ser. No. 13/299,120, filed Nov. 17, 2011, now issued as U.S. Pat. No. 8,555,495, which is a divisional of U.S. application Ser. No. 12/705,923, filed Feb. 15, 2010, now issued as U.S. Pat. No. 8,065,792, which is a divisional of U.S. application Ser. No. 10/744,632, filed Dec. 23, 2003, now issued as U.S. Pat. No. 7,712,211, which claims priority under Title 35, USC 119, to Singapore Application No. 200302511-1, filed May 6, 2003, all of which are incorporated in their entirety herein by reference.

TECHNICAL FIELD

The present invention relates generally to circuit packaging, and in particular to apparatus and methods for packaging integrated circuits.

BACKGROUND

Wafers are fabricated with a plurality of dies each having a plurality of integrated circuit elements therein. A die represents one individual chip that must be separated from adjacent dies before packaging. Contacts are added to the die before packaging. One type of contact is a bond pad. Wafer level packaging (WLP) refers to the integrated circuit packaging formed at the wafer level, usually at the wafer foundry. WLP is normally considered as a true chip size package. WLP thus provides lower cost and smallest size of commercial packaging. It is desired to reduce the profile and/or thickness of packaged components using a commercially viable process.

For the reasons stated above, for other reasons stated below, and for other reasons which will become apparent to those skilled in the art upon reading and understanding the present specification, there is a need in the art for an improved electronic component package and methods of packaging electronic components.

SUMMARY

The present invention is directed to forming a wafer-scale, integrated circuit package. That is, the present invention is directed to chip-scale packages An embodiment of the present invention includes fixing a die on a substrate, forming electrical connections from die to terminals on the substrate, and removing a backside of substrate to expose the terminals. In an embodiment, removing the backside of the substrate includes backgrinding the substrate to expose a backside of the terminals. In an embodiment, fixing the die to the substrate includes applying an adhesive to the top surface of the substrate and placing the die on the adhesive. The adhesive is cured to fix the die to the substrate. In an embodiment, the die is placed vertically over the terminals for that die. The electrical connections are formed from the die through the adhesive layer to the terminals. In an embodiment, the terminals are conductive pads formed on the top surface of the substrate. In an embodiment, the electrical connections are metal traces from the die to the conductive pads. In an embodiment, the adhesive layer is removed from around the periphery of the die to expose the terminals. In an embodiment, terminals on the substrate are interconnected to provide greater functionality of chip-scale package. In an embodiment, the die is singulated from adjacent die with a portion of the substrate remaining with the die. The singulated die package forms individual chip scale packages that include at least one active device and a portion of the second substrate.

An embodiment of the present invention further provides the ability to expand the functionality of the present invention to a multi-chip module. Dice are fixed to a substrate, for example, as described above and further described below. The gaps between the die are filled with an insulator. In an embodiment, the insulator is a rigid material, when cured, to assist in the mechanical strength of the multi-chip module. In an embodiment, terminals in the substrate are electrically connected to provide inter-chip electrical communication. This expands the functionality of them multi-chip module. In an embodiment, the dice in the multi-chip module each include an integrated circuit memory. In an embodiment, a first die includes an integrated circuit memory and a second die includes an integrated circuit. In an embodiment, the second die includes a processor. In an embodiment, the second die includes logic circuits.

An embodiment of the present invention includes fixing an active device substrate that has a plurality of dice to a base substrate. Electrical communication lines are formed between the die and respective package level terminals or pads on the base substrate. The backside of the base substrate remote from the active device substrate is removed to expose the package level terminals. The dice are separated with its respective portion of the base substrate, which at least partially includes package level terminals. In an embodiment, a top surface of the base substrate is coated with an adhesive. In an embodiment, the removing the backside of the base substrate includes back grinding the base substrate. In an embodiment, separating the dice includes singulation, for example by laser. In an embodiment, forming electrical connections includes forming a conductive trace from a top bond pad of a die along the side of the die to contact a package level terminal. In an embodiment, the conductive trace is formed by a metal redistribution process.

An embodiment of the present invention is directed to a chip-scale-packaging method including fixing two substrates together and forming electrical contacts between active devices on the two substrates. In an embodiment, the two substrates each include a plurality of dice that contain the active integrated circuits. The dice are singulated to form discrete packages with contacts on each die and along the sides of the package. In an embodiment, fixing the two substrates together includes coating the top surface of the second substrate with an adhesive and curing the adhesive to fix the second substrate on the first substrate. In an embodiment, the first substrate is placed on the adhesive layer such that the saw streets of the first substrate align with the saw streets of the second substrate. In an embodiment, a plurality of through apertures are formed in the aligned first and second saw streets. The electrical connections from the first dice on the first substrate are formed through the through apertures to the second dice on the second substrate. In an embodiment, forming electrical connections from the first dice on the first substrate to the second dice on the second substrate includes routing a conductive trace from a first bond pad on an active device surface of the first substrate to a second bond pad on an active device surface of the second substrate through the through aperture. In an embodiment, singulating dice includes mechanically cutting the saw streets. In an embodiment, singulating dice includes lazing the saw streets. In an embodiment, cutting the saw streets includes partially cutting the electrical connection in the through apertures such that a portion of the electrical connection in a specific through aperture remains with each of

the dice adjacent the through aperture. In an embodiment, forming electrical connections includes forming metal traces including at least one metal from a group consisting essentially of copper and aluminum. In an embodiment, forming through apertures and/or cutting the saw streets include cutting a kerf in at least one of the saw streets

Embodiments of the present invention further include connecting the chip-scale package to a further substrate such as a circuit board. The chip-scale-package of an embodiment of the present invention includes contacts at the top of the die, along the side of the die and at the terminals formed in the substrate.

The present invention also includes substrates, wafers, integrated circuit packages, electrical devices, memory devices, memory units, memory modules, electrical systems, computers, which include a chip-scale-package according to the present invention.

These and other embodiments, aspects, advantages, and features of the present invention will be set forth in part in the description which follows, and in part will become apparent to those skilled in the art by reference to the following description of the invention and referenced drawings or by practice of the invention. The aspects, advantages, and features of the invention are realized and attained by means of the instrumentalities, procedures, and combinations particularly pointed out in the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a flow chart of a method according to an embodiment of the present invention.

FIG. **2** is a plan view of a substrate during a method step according to the teachings of the present invention.

FIG. **3** is a cross-sectional view taken generally along line **3-3** of FIG. **2**.

FIG. **4** is a further cross-sectional view after s further method step according to the teachings of the present invention.

FIG. **5** a plan view of a substrate during a method step according to the teachings of the present invention.

FIG. **6** is a cross-sectional view taken generally along line **6-6** of FIG. **5**.

FIG. **7** is an enlarged cross-sectional view taken generally along line **7-7** of FIG. **5**.

FIG. **8** is a cross-sectional view of during a method step according to the teachings of the present invention.

FIG. **9** is a cross-sectional view of during a method step according to the teachings of the present invention.

FIG. **10** is a cross-sectional view of during a method step according to the teachings of the present invention.

FIG. **11** is a cross-sectional view of during a method step according to a multi-chip package of the present invention.

FIG. **12** is a cross-sectional view of during a method step according to the multi-chip package according to the teachings of the present invention.

FIG. **13** is a cross-sectional view of an electrical system according to the teachings of the present invention.

FIG. **14** is a flow chart of a method according to an embodiment of the present invention.

FIG. **15** is an elevational view of an embodiment of the present invention.

FIG. **16** is a fragmentary top view after a step according to an embodiment of the present invention.

FIG. **17** is a fragmentary top view after a step according to an embodiment of the present invention.

FIG. **18** is a cross-sectional view taken generally along line **18-18** of FIG. **17**.

FIG. **19** is a schematic view of a die stack according to the embodiment shown in FIGS. **15-18**.

FIG. **20** is a view of a circuit module according to the teachings of the present invention.

FIG. **21** is view of a memory module according to the teachings of the present invention.

FIG. **22** is a view of an electronic system according to the teachings of the present invention.

FIG. **23** is a view of an embodiment of an electronic system according to the teachings of the present invention.

FIG. **24** is a view of a computer system according to the teachings of the present invention.

DETAILED DESCRIPTION OF THE EMBODIMENTS

In the following detailed description of the embodiments, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration specific embodiments in which the inventions may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilised and that process, electrical or mechanical changes may be made without departing from the scope of the present invention. The terms wafer and substrate used in the following description include any base semiconductor structure. Both are to be understood as including silicon-on-sapphire (SOS) technology, silicon-on-insulator (SOI) technology, thin film transistor (TFT) technology, doped and undoped semiconductors, epitaxial layers of a silicon supported by a base semiconductor structure, as well as other semiconductor structures well known to one skilled in the art. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims and their equivalents.

The present description uses the relative terms Atop@ and Aback@ when referring to the substrate on which integrated circuits are formed. The term Atop@ herein refers to the surface on which the layers that form an active integrated circuit structure are fabricated. The term Aback@ herein refers to the region of the substrate beneath the surface on which active circuit structures are fabricated.

FIG. **1** shows a flowchart of a method for packaging according to an embodiment of the present invention. The method is generally directed to wafer level packaging that achieves a chip scale package. A plurality of dies are formed on a top surface of a substrate, **101**. One type of a substrate is a wafer. The wafer is crystalline silicon in an embodiment. Each die includes an active integrated circuit such as a memory device, processor, logic circuits, or application specific integrated circuits. Memory devices include read only memory, dynamic random access memory, static random access memory, EEPROM, and flash memory. Additionally, the memory device could be a synchronous memory device such as SGRAM (Synchronous Graphics Random Access Memory), SDRAM (Synchronous Dynamic Random Access Memory), SDRAM II, and DDR SDRAM (Double Data Rate SDRAM), as well as Synchlink or Rambus DRAMs and other emerging memory technologies as known in the art. Such active devices are tested to identify and remove faulty active devices from further fabrication and to identify possible error-inducing fabrication processes, **103**. The dice are singulated from each other, **105**. In an embodiment, the testing occurs at the wafer level prior to

singulation. The dice identified as good dice are selected and ready for further fabrication and/or packaging.

A base substrate is formed separately from the active die substrate. The base substrate is adapted to provide electrical communication terminals for the active dice in a wafer level package. The base substrate is composed of a non-conductive material. In an embodiment, the base substrate is crystalline silicon. In an embodiment, the base substrate is a wafer. Package level terminals are formed on a top surface of the base substrate, **107**. Such package level terminals are patterned, discrete conductive pads. In an embodiment, the package level terminals are formed of a metal. In an embodiment, the metal is copper. In an embodiment, the metal is aluminum. If electrical communication is required between the package level terminals, then conductive lines or traces are formed on the base substrate between the package level terminals, **109**.

The top surface of the base substrate is coated with an adhesive, **111**. In an embodiment, the adhesive is spin coated on the base substrate top surface. In an embodiment, the adhesive is pattern coated on the base substrate top surface. Examples of patterning the adhesive include screen printing and jet printing. The adhesive includes a polymide (PI) in an embodiment. The adhesive includes a benzocyclobutene (BCB) in an embodiment.

The singulated dice are picked and placed on the adhesive layer generally over the package level terminals, **113**. The adhesive is cured to fix the dice to the base substrate. In an embodiment with the adhesive covering the package level terminals, the adhesive is removed from over at least a portion of the package level terminals. That is, the package level terminals extend outwardly from the footprint of the die. Thus, the adhesive that is not beneath the die is at least partially removed to expose a portion of the terminal.

Conductive lines are formed from the input/output pads of the dice to the package level terminals, **115**. The die input/output pads are on the top surface. The conductive lines extend outwardly from the die input/output pads and down the side of the die through the adhesive layer to physically and electrically contact the package level terminals. In an embodiment, the conductive lines include castellation lines. In an embodiment, the conductive lines are formed by a redistribution layer process. The redistribution layer process includes blanket depositing a metal redistribution layer on the die and on at least the package level terminals of the base substrate. Next, a radiant sensitive film, such as a wet film resist, or a dry film resist, is blanket deposited on the redistribution layer. The radiant sensitive film is then exposed to a radiant source, e.g., a light source or laser, to the pattern of conductor lines. Development of the exposed radiant sensitive film forms a mask that can be used to etch the pattern of conductor lines. Such an etching process is known in the art as a "subtractive" process. An Aadditive@ process could also be used where the mask is patterned and then the conductor for the redistribution layer is deposited in the spaces in the mask. The mask and any conductive material on the mask is then removed. In an embodiment, the conductive material for the conductive lines is a metal. In an embodiment, the metal includes copper. In an embodiment, the metal includes aluminum.

In an embodiment of the present invention, a plurality of the die remain joined on the base substrate to form a multi-chip module. Such a multi-chip module increases the functionality of the individual die. For example, different types of integrated circuits are in different die in the multi-chip module such as logic circuits or processors and memory devices. The gaps between the die on the base substrate are filled with a non-conductive material, **117**. This increases the mechanical strength of the multi-chip module.

The backside of the package level terminals remain covered by the backside of the base substrate. The backside of the base substrate is removed, **119**, to expose the back of the package level terminals, which are connected to a die input/output pad through the conductive lines. In an embodiment, either a wet or dry etching process can be used to etch the backside of the substrate to form a thinned substrate. For thinning by wet etching, an etchant solution containing a mixture of KOH (Potassium Hydroxide) and H_2O can be utilized. A one to one solution at a temperature of about 60 degrees to 80 degrees C. will etch monocrystalline silicon at an etch rate of about 300 to 800 angtroms/min. Another wet etching process can be performed using an isotropic etch of HNO_3 and HF producing an etch rate of 55-60 Φm/min. A dry etch process with an etchant such as a species of chlorine can also be utilized. In this case, the etch rate will be much slower than specified above. Alternately, thinning can be performed using chemical mechanical polishing (CMP). CMP includes a mechanical pad and a silica based slurry composition to back polish or back grind the substrate without chemical etching. The back surface of the package level terminals are now exposed.

A very thin sliver of the base substrate remains connecting the package level terminals to each other. This remaining base substrate sliver is cut to singulate the wafer level packages, **121**, which include a die and a portion of the base substrate and portions of the package level terminals. Each packaged die is singulated from the other packaged dies in an embodiment. In an embodiment, a plurality of die remain together to form a multi-chip module that is singulated from other die and/or other multi-chip modules.

In an embodiment, the singulated die or singulated multi-chip modules are attached to a further electronic base, **123**. One type of electronic base is a circuit board such as a PCB. The exposed package level terminals are electrically connected to conductors, such as land patterns, on the further electronic base. In an embodiment, the singulated die or multi-chip module are fixed to a further electronic base using surface mount technology.

FIG. **2** shows a plan view of an active device substrate **200**. As shown the substrate **200** is a wafer, however, the present invention is not limited to only a wafer. A plurality of input/output or bond pads **202** are on the top surface of the individual die that include active devices and are formed on the substrate **200**. FIG. **2** shows a schematic representation of the position of pads **202** to better illustrate the present invention. It will be recognized that the bond pads **202** are typically much smaller and greater in number with respect to the substrate **200**. An array of bond pads **204** define an attachment location **206** for a die. The bond pad array **204** provides the external, backside connections for an attached die. Conductive traces **208** are formed in the substrate **200** between certain bond pads **202** in an embodiment. The traces **208** provide electrical communication lines between bond pad arrays, e.g., trace **208**B connecting a pad in array **204**B to a pad in array **204**C, trace **208**C connecting a pad in array **204**C to a pad in array **204**D, and trace **208**E connecting a pad in array **204**D to a pad in array **204**E. The traces **208** can also connect pads with an array, e.g., trace **208**D connecting two pads together in array **204**D.

FIG. **3** shows a cross sectional view of substrate **200** taken generally along line **3-3** of FIG. **2**. A base layer **210** is provided. In an embodiment, the base layer is a bare wafer. In an embodiment, the base layer is formed of monocrystalline silicon. A plurality of conductive bond pads **202** are

formed on the top surface of the substrate **210**. In an embodiment, the bond pads **202** include metal. In an embodiment, the bond pads are aluminum. In an embodiment, the bond pads are copper. The bond pads **202** are separated by insulative material **211**. In an embodiment, the insulative material is silicon dioxide. The top surface **212** of substrate **200** is essentially planar. In an embodiment, the top surface **212** is planarized after the bond pads **202** are formed. Planarizing the top surface **212** may include chemical-mechanical polishing.

FIG. **4** shows a cross sectional view of substrate **200** after a further process step of the present invention. An adhesive layer **214** is deposited on the surface **212**. The adhesive layer **214** is spin coated on substrate **200**. The adhesive layer **214** covers the entire surface **212**. In an embodiment, the adhesive layer includes a polymide. In an embodiment, the adhesive layer includes benzocyclobutene (BCB). In an embodiment, the adhesive layer **214** is patterned such that it covers at least the attachment locations **206** for the die. The adhesive layer **214** could be patterned by printing techniques.

FIG. **5** shows a fragmentary plan view of substrate **200** after a further process step. A plurality of die **215**, which include active devices such as integrated circuits, are fixed to the attachment locations **206** by adhesive layer **214** to form a dice/substrate assembly **220**. Each die **215** includes a plurality of die bond pads **217** on top of the die and in electrical communication with the active devices in the die. The die bond pads **217** provide electrical contacts for the active devices and electrical circuits outside the die.

Referring now to FIGS. **6** and **7**, FIG. **6** shows a cross sectional view taken generally along line **6-6** in FIG. **5**. FIG. **7** shows a cross sectional view taken generally along lin **7-7** of FIG. **5** and with an increased scale. FIGS. **6** and **7** show the assembly **220** of dice **215** with the base substrate **200**. The dice **215** are pressed onto the adhesive layer **214**. Adhesive layer **214** is cured to fix the dice **215** to the base substrate **200**. FIG. **8** shows a view similar to FIG. **7** after a further process step of removing the adhesive layer **214** except the portion of adhesive layer fixing the dice **215** to substrate **200**. The adhesive is selectively removed from on top of portions of wafer level terminals **202** to thereby create trenches **221** extending from the top of dice **215** to the top surface of terminals **202**. FIG. **9** shows a view similar to FIG. **8** of assembly **220** after a further process step of forming a redistribution layer. The redistribution layer forms conductive lines **223** from the die pads **217** to the wafer level terminals **202**. FIG. **10** shows a view similar to FIG. **9** of assembly **220** after a further process step of singulating the assembly **220** into wafer level packages **220**A and **220**B. This singulation step is accomplished by mechanically cutting through the insulative layer **211** and the wafer level terminals **202** that are intermediate the dice **215**. In an embodiment, a saw blade is used to mechanically cut the die from each other. In an embodiment, a laser is used to mechanically cut the die from each other. In an embodiment, a laser/water jet is used mechanically cut the die from each other. An embodiment of the laser/water jet is described in U.S. patent application Ser. No. 10/118,666, titled A WAFER DICING DEVICE AND METHOD@ and having the same assignee as the present application, which application is incorporated herein by reference for any purpose. The singulated wafer level packages now have electrical contacts on the back surface, i.e., the wafer level terminals **202**; on the top surface, i.e., the top portion of conductive line **223** and/or bond pad **217**; and on the side surface, i.e., the conductive line **223**. These singulated wafer level packages **220**A and **220**B could now be stacked on top of each other or contact other circuits on one, two or, three sides to improve the functionality of the active circuit within the wafer level package **220**A, **220**B.

FIG. **11** shows an alternate embodiment of the present invention. An assembly **220** is prepared as describe above through FIG. **9**. After the conductive lines **223** are formed, the trenches **221** are filled with a non-conductive layer **227**. Dice connected physically together by layer **227** remain together as a multi-chip module. In an embodiment, the trench filling material of layer **227** includes a polymide (PI). The trench filling material of layer **227** includes a benzocyclobutene (BCB) in an embodiment. After layer **227** is formed the backside of substrate **200** is removed (FIG. **12**). A wafer level package **220**C is formed. It will be recognized that layer **227** covers the top portion of dice **215** in an embodiment. In an embodiment, layer **227** only filles the trenches **221** leaving the top of conductive lines **223** and bond pads **217** exposed and available to connect to external electrical circuits.

FIG. **13** shows a final assembly **230** including a wafer level package **220**A of the present invention. A wafer level package **220**A is mounted to an electrical system substrate **231** using surface mount technology. In an embodiment, substrate **231** is a PCB. Electrical system substrate **231** includes a plurality of land contacts **233**. The plurality of land contacts **233** are covered by a conductive solder **234**. Wafer level terminals **202** of wafer level package **220**A are placed on the solder **234**. The solder **234** is cured to mechanically and electrically connect wafer level package **220**A to substrate **231**. While shown and described with a single die wafer level package **220**A, the same assembly is used for a multi-chip module **220**C which would require additional contacts.

FIG. **14** shows a flowchart of a method for packaging according to an embodiment of the present invention. Processes **101**, **103**, **107**, **109** and **111** are the same as those described above with reference to FIG. **1**. The active device die are not singulated in this embodiment prior to adhering the active device substrate to the base substrate. This embodiment includes bonding the active device substrate to the base substrate. **330**. An embodiment includes joining a wafer containing the active devices to a base wafer that includes the wafer level terminals and is coated with an adhesive layer. The adhesive is cured. The active device substrate is then cut to a depth at least equal to the height of the active device substrate, **332**. An example of this type of partial cutting (creating kerfs) is described in U.S. patent application Ser. No. 10/232,226, titled A WAFER LEVEL PACKAGING@, filed Aug. 28, 2002, and incorporated by reference herein for any purpose. The active device dies are now separated by trenches. The adhesive that remains at the bottom of the trench on the base substrate and not under the die of the active device is removed to expose the wafer level terminals. Conductive lines are formed from the input/output pads of the dice to the package level terminals, **115**. The die input/output pads are on the top surface. The conductive lines extend outwardly from the die input/output pads and down the side of the die through the adhesive layer to physically and electrically contact the package level terminals. In an embodiment, the conductive lines include castellation lines. In an embodiment, the conductive lines are formed by a redistribution layer process. The package level terminals remain covered by the backside of the base substrate. The backside of the base substrate is removed, **119**, to expose the back of the package level terminals, which are connected to a die input/output pad through the

conductive lines. In an embodiment, either a wet or dry etching process can be used to etch the backside of the substrate to form a thinned substrate. Alternately, thinning can be performed using chemical mechanical polishing (CMP). CMP includes a mechanical pad and a silica based slurry composition to back polish or back grind the substrate without chemical etching. The back surface of the package level terminals are now exposed. Other mechanically grinding processes related to integrated circuit processes are within the scope of the present invention. The dice/base substrate is now singulated, **121**. If needed the singulated dice with a portion of the base substrate is connected to a further electronic substrate, **123**.

FIGS. **15-19** show a further embodiment of the present invention. In this embodiment, two substrates **300** each having active devices formed on an respective, active side are joined togther at the substrate level. In an embodiment, both substrates **300** are wafers and are joined together at the wafer level. Each substrate **300** includes a substrate base layer **350** on which is formed an active device layer **352**. The substrate base layer **350** is monocrystalline silicon in an embodiment. The active areas **352** each include a plurality of die **315** that include the active circuits electrically connected to bond pads **317**. Dice **315** are substantially similar to dice **215** described herein. Bond pads **317** are substantially similar to bond pads **217** described herein. The bond pads **317** are formed on the top of the dice **315** remote from the substrate base layer **350**. Individual die are separated from each other by saw streets **355**. The top and bottom substrates **300** are mirror images of each other so that corresponding die **315** in each of the top and bottom substrate **300** align with each other as well as the saw streets **355** aligning with each other. The saw streets **355** of the top substrate would lie directly above the saw streets **355** of the bottom substrate. In joining the top substrate to the bottom substrate, the bottom substrate is flipped so that its backside **357** faces upward. The backside **357** of the bottom substrate **300** is coated with an adhesive **314**. Adhesive **314** is substantially similar to adhesive **214** described herein. Backside **357** of the top substrate is brought into contact with the adhesive **314**. The adhesive is cured to fix the substrates together. The saw streets **355** are vertically aligned. A plurality of through vias or apertures **360** are formed in the saw streets through both the top substrate and the bottom substrate. Vias **360** are formed by lazing the saw streets to burn through the two substrates **300** and the adhesive layer **314**. In an embodiment, the laser is adapted for cutting substrate structures fabricated according to known techniques. In an embodiment, the laser is a solid state laser. In an embodiment, the laser is a yttrium-aluminum-garnet (YAG) laser. In an embodiment, the laser is a neodymium-YAG laser. The laser wavelength, in an embodiment, is about 1 micrometer. In an embodiment, the laser power is about 300 watts. In an embodiment, the laser power is less than about 300 watts. In an embodiment, the laser power is greater than about 100 watts. In an embodiment, the laser refresh rate is about 3,000 Hz. In an embodiment, the laser refresh rate is less than about 3,000 Hz. In an embodiment, the laser refresh rate is greater than 1,000 Hz. In an embodiment, the laser is an excimer laser. The laser is desirable for use in scribing or cutting the workpiece (here, the stacked substrates **300**) as the laser does not apply mechanical stress onto the workpiece. A plurality of conductive lines **323** are formed from the top die bond pads **317** to the edge of the die and through a respective via **360** to the bottom die bond pads **317** (FIGS. **17** and **18**). The conductive lines **323** are formed by a redistribution layer process as described herein. Conductive lines **323** are substantially similar to conductive lines **232**. Now the vertically aligned dice that are joined by the adhesive are electrically connected togther through a conductive line **323**. The individual joined die assembly **365** can now be singulated. Singulated die assembly **365** are schematically shown in FIG. **19** with the conductive line **323** remaining in part of via **360** after cutting the adjacent die assemblies apart during singulation.

Circuit Modules

As shown in FIG. **20**, two or more substrate level packaged dice **2001** of the present invention may be combined, with or without protective casing, into a circuit module **2000** to enhance or extend the functionality of an individual die **2001**. Circuit module **2000** may be a combination of dies **2001** representing a variety of functions, or a combination of dies **2001** containing the same functionality. In an embodiment, circuit module **2000** includes at least one socket, slot, recess or the like **2052** into which the die **2001** is received. One or more dies **2001** of circuit module **2000** include I/O structures in accordance with the invention and/or are fabricated in accordance with the present invention. In an embodiment, dies **2001** are inserted into a slot **2052** in a circuit board **2050** such that the package level terminals **202** or conductive traces **323** are in electrical communication with the contacts in the slot **2052**. In an embodiment, package level terminals **202** or conductive traces **323** are in physical contact with contacts in the slot **2052**. In an embodiment, the contacts package level terminals **202** or conductive traces **323** are press fit into the slot **2052** against the contacts of the slot.

Numeral **2052** in FIG. **20**, in another embodiment, represents a mount including land patterns whereat the contacts according to the present invention are mounted. The mounting process includes an SMT process. For example, circuit module **2000** is a printed circuit board having land patterns on which solder paste is applied, e.g., by printing the solder paste. A substrate level packaged die **2001** of the present invention is picked and placed at the mount with the package level terminals **202** or conductive traces **323** aligned with the paste covered contacts of the mount. Either the package level terminals **202** or conductive traces **323** or the mount contacts are reflowed to create a physical and electrical connection.

Some examples of a circuit module include memory modules, device drivers, power modules, communication modems, processor modules and application-specific modules, and may include multilayer, multichip modules. Such modules will have a chip receiver in which a chip according to the present invention is inserted. Circuit module **2000** may be a subcomponent of a variety of electronic systems, such as a clock, a television, a cell phone, a personal computer, an automobile, an industrial control system, an aircraft and others. Such modules will have a circuit module receiver in which a circuit module according to the present invention is inserted. Circuit module **2000** will have a variety of leads $\mathbf{2005}_1$ through $\mathbf{2005}_N$ extending therefrom and coupled to the package level terminals **202** or conductive traces **323** of substrate level packaged dice **2001** providing unilateral or bilateral communication and control.

FIG. **21** shows one embodiment of a circuit module as memory module **2100**. Memory module **2100** contains multiple memory devices **2101** contained on support **2161**. In an embodiment, support **2161** includes slots **2152** for receiving memory devices **2101** as described herein. The number of memory devices generally depends upon the desired bus width and the desire for parity. Memory devices **2101** include at least die in accordance with to the present

invention. The support **2161** includes sockets, slots, recesses or the like **2152**, each adapted to receive a memory device **2101** and provide electrical communication between a bus and memory device **2101**. Memory module **2100** accepts a command signal from an external controller (not shown) on a command link **2163** and provides for data input and data output on data links **2165**. The command link **2163** and data links **2165** are connected to leads **2167** extending from the support **2161**. Leads **2167** are shown for conceptual purposes and are not limited to the positions shown in FIG. **21**.

Electronic Systems

FIG. **22** shows an embodiment of an electronic system **2200** containing one or more circuit modules **2000**. At least one of the circuit modules **2000** contains a die in accordance with the present invention. Electronic system **2200** generally contains a user interface **2269**. User interface **2269** provides a user of the electronic system **2200** with some form of control or observation of the results of the electronic system **2200**. Some examples of user interface **2269** include the keyboard, pointing device, monitor or printer of a personal computer; the tuning dial, display or speakers of a radio; the ignition switch, gauges or gas pedal of an automobile; and the card reader, keypad, display or currency dispenser of an automated teller machine. User interface **2269** may further describe access ports provided to electronic system **2200**. Access ports are used to connect an electronic system to the more tangible user interface components previously exemplified. One or more of the circuit modules **2000** may be a processor providing some form of manipulation, control or direction of inputs from or outputs to user interface **2269**, or of other information either preprogrammed into, or otherwise provided to, electronic system **2200**. In an embodiment, electronic system **2200** includes memory modules **2100**. As will be apparent from the lists of examples previously given, electronic system **2200** will often be associated with certain mechanical components (not shown) in addition to circuit modules **2000** and user interface **2269**. It will be appreciated that the one or more circuit modules **2000** in electronic system **2200** can be replaced by a single integrated circuit. Furthermore, electronic system **2200** may be a subcomponent of a larger electronic system.

FIG. **23** shows one embodiment of an electronic system as memory system **2300**. Memory system **2300** contains one or more memory modules **2100** and a memory controller **2370**. At least one of the memory modules **2100** includes a die in accordance with the present invention. Memory controller **2370** provides and controls a bidirectional interface between memory system **2300** and an external system bus **2372**. Memory system **2300** accepts a command signal from the external bus **2372** and relays it to the one or more memory modules **2100** on a command link **2374**. Memory system **2300** provides for data input and data output between the one or more memory modules **2100** and external system bus **2372** on data links **2376**.

FIG. **24** shows a further embodiment of an electronic system as a computer system **2400**. Computer system **2400** contains a processor **2401** and a memory system **2300** housed in a computer unit **2480**. In an embodiment, the memory system **2300** includes a die in accordance with the present invention. In an embodiment, processor **2401** includes a die in accordance with the present invention. In an embodiment, the memory system and processor dies are combined according to the present invention. Computer system **2400** is but one example of an electronic system containing another electronic system, i.e., memory system **2300**, as a subcomponent. Computer system **2400** optionally contains user interface components. Depicted in FIG. **11** are a keyboard **2481**, a pointing device **2483** such as a mouse, trackball, or joystick, a monitor **2485**, a printer **2487** and a bulk storage device **2489**. It will be appreciated that other components are often associated with computer system **2400** such as modems, device driver cards, additional storage devices, etc. These other components, in an embodiment, include a die in accordance with the present invention. It will further be appreciated that the processor **2401** and memory system **2300** of computer system **2400** can be incorporated on a single integrated circuit. Such single package processing units reduce the communication time between the processor and the memory circuit.

CONCLUSION

It is desired to reduce the size of packaged components. This results in packaging material savings and increases throughput by reducing packaging fabrication times. Moreover, with the growing popularity of smaller electronic device the electronic components must be as small as possible. The present invention further provides methods for producing a packaged die. In an embodiment, dice are fixed on a base substrate that has contacts or terminals formed thereon. The dice are electrically connected to the terminals. For example, top level I/O pads of the dice are connected to the terminals by conductive traces running from the top of the dice along its side to the terminals below the dice. The backside of the base substrate is removed to expose the backside of the terminals thereby forming a true chip-size package. The die can now be singulated. This process can be performed at the wafer foundry thereby increasing fabrication throughput. Wafer foundries have fabrication and substrate handling equipment to facilitate the present process.

Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement which is calculated to achieve the same purpose may be substituted for the specific embodiments shown. Many adaptations of the invention will be apparent to those of ordinary skill in the art. For example, other integrated circuit processing equipment may be utilised in conjunction with the invention. For another example, other integrated circuit fabrication processes are adapted to produce the dies and chips according to the present invention. Accordingly, this application is intended to cover any adaptations or variations of the invention. It is manifestly intended that this invention be limited only by the following claims and equivalents thereof.

The invention claimed is:

1. A chip-scale-packaging method, comprising:

singulating a die from a first wafer;

testing the singulated die;

forming final I/O locations on a second wafer;

applying adhesive to a top surface of the second wafer;

placing the singulated die on the adhesive over the final I/O locations;

removing a back surface of the second wafer to expose the final I/O locations; and

connecting the singulated die to an electric circuit through the final I/O location,

wherein singulating the die from the first wafer includes mechanically cutting saw streets to form a side of the first and second wafers, and wherein singulating the die includes exposing at least one electrical connection along the side of the first and second wafers.

2. The chip-scale-packaging method of claim **1**, wherein removing the back surface of the second wafer includes backgrinding the second wafer.

3. The chip-scale-packaging method of claim 1, wherein removing the back surface of the second wafer includes etching the back surface of the second wafer.

4. The chip-scale-packaging method of claim 1, wherein removing the back surface of the second wafer includes separating the singulated die and a portion of the second wafer from a remainder of the second wafer.

5. The method of claim 1, wherein removing the back surface of the second wafer includes backgrinding the second wafer.

6. The method of claim 1, wherein removing the back surface of the second wafer includes etching the back surface of the second wafer.

7. A chip-scale-packaging method, comprising:

singulating a die from a first wafer;

testing the singulated die;

forming final I/O locations on a second wafer;

applying adhesive to a top surface of the second wafer;

placing the singulated die on the adhesive over the final I/O locations;

removing a back surface of the second wafer to expose the final I/O locations; and

connecting the singulated die to an electric circuit through the final I/O location,

wherein singulating the die includes exposing at least one electrical connection along a side of the first and second wafers.

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